CLAIM LISTING

This listing of claims will replace all prior versions, and listings of claims in the application:

IN THE CLAIMS

1. (Previously Presented) In an integrated circuit, a layer including a plurality of conductive wires, the layer comprising:

a horizontal surface of a first wire of the plurality of conductive wires having a proximal end and a distal end, the proximal end having a first width, the distal end having a second width, the second width being less than the first width, the first wire tapered from the proximal end to the distal end, the first wire further having a first substantially vertical surface;

a second wire of the plurality of conductive wires spaced apart from the first wire, the second wire having a second substantially vertical surface, the first wire and the second wire each horizontally disposed along side each other, wherein capacitors are created between the first substantially vertical surface and the second substantially vertical surface, the capacitors respectively associated with capacitances, the capacitors being associated with a plurality of loads, the plurality of loads being progressively reduced responsive to a progressive reduction of the capacitances as associated with the first wire taper; and

a plurality of taps, a tap of the plurality of taps located between a pair of loads of the plurality of loads.

2. (Original) The layer, according to claim 1, further comprising at least one dielectric material disposed between the first substantially vertical surface and the second substantially vertical surface.

3. (Original) The layer, according to claim 1, wherein the first wire is a signal wire.

4. (Original) The layer, according to claim 3, wherein the second wire is a shielding wire.

5. (Original) The layer, according to claim 4, wherein the first wire is tapered in progressively inward stepwise indentations away from the second wire along the first substantially vertical surface.

6. (Original) The layer, according to claim 5, wherein the first wire is tapered in progressively inward stepwise indentations toward the second wire along another substantially vertical surface of the first wire.

7. (Original) The layer, according to claim 1, wherein the first wire is a shielding wire, the shielding wire for a non-transitioning signal voltage, the non-transitioning signal voltage not transitioning from high-to-low and low-to-high logic levels during application of electrical energy to operate the integrated circuit.

8. (Original) The layer, according to claim 7, wherein the second wire is a signal wire, the signal wire for a transitioning signal voltage, the transitioning signal voltage transitioning from high-to-low and low-to-high logic levels during application of the electrical energy to operate the integrated circuit.

9. (Original) The layer, according to claim 8, wherein the first wire is continuously tapered away from the second wire along the first substantially vertical surface.

10. (Original) The layer, according to claim 8, wherein the first wire is continuously tapered toward the second wire.

11. (Previously Presented) An integrated circuit conductive line, comprising:

a plurality of loads, the plurality of loads progressively reduced responsive to progressively reduced parasitic capacitance;

the plurality of loads being provided using a first wire and a second wire, at least one of the first wire and the second wire selected from a group consisting of a tapered signal line and a tapered shielding line;

a dielectric layer located between the first wire and the second wire;

the progressively reduced parasitic capacitance responsive to a lengthwise tapering of at least one of the first wire and the second wire; and

a plurality of taps, a tap of the plurality of taps located between a pair of loads of the plurality of loads.

12. (Original) The integrated circuit conductive line, according to claim 11, wherein load capacitance at the tap is substantially less than the parasitic capacitance at the tap location from a portion of the plurality of loads.

13. (Original) The integrated circuit conductive line, according to claim 12, wherein the load capacitance comprises transistor gate capacitance.

14. (Original) The integrated circuit conductive line, according to claim 13, wherein the transistor gate capacitance is from a transistor formed with sub-quarter micron lithography.

15. (Cancelled)

16. (Previously Presented) The integrated circuit conductive line, according to claim 11, wherein the tapered signal line has a minimum width of one micron.

17. (Previously Presented) The integrated circuit conductive line, according to claim 11, wherein the tapered signal line is a clock signal line.

18. (Previously Presented) The integrated circuit conductive line, according to claim 11, wherein the tapered signal line is a delay line.

19. (Cancelled)

20. (Original) The integrated circuit conductive line, according to claim 11, wherein the tapered shielding line is either a ground line or a source voltage line.

21.-27. (Cancelled)